



Princess Sumaya University For Technology

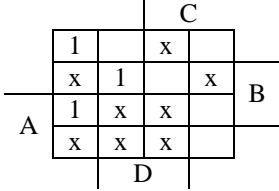
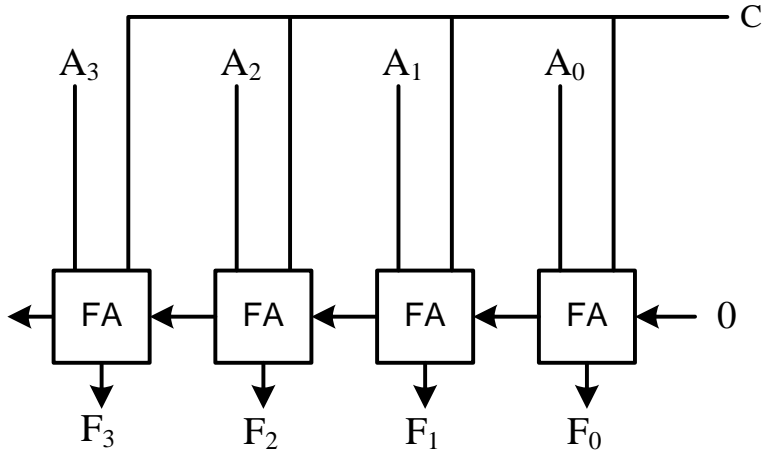
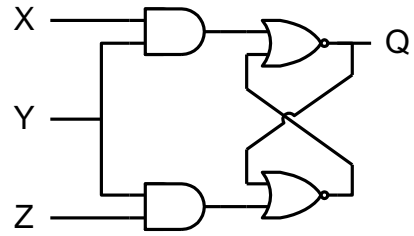
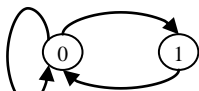
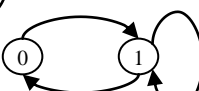
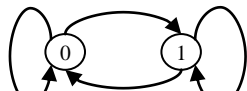
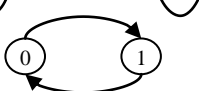
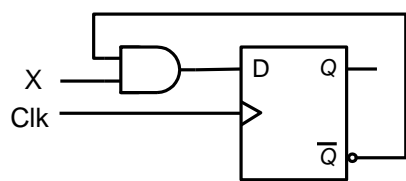
Computer Engineering Dept.

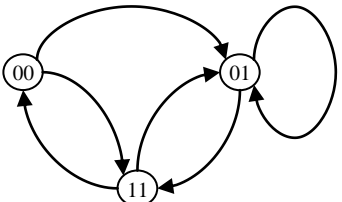
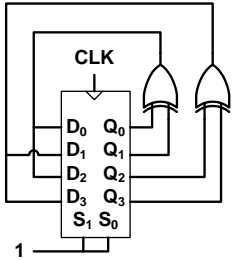
4241 - Digital Logic Design

Sample Final Exam

Dr. B. Kahhaleh

Problem 1 (1 Point)	<p>Given the numbers $(1000100)_2$, $(1000003)_8$, $(1000002)_{10}$, $(1000001)_{16}$:</p> <ul style="list-style-type: none"> a) They all have the same value b) $(1000100)_2$ is the smallest c) $(1000002)_{10}$ is the biggest d) $(1000100)_2$, $(1000003)_8$, and $(1000001)_{16}$ have equal value and different than $(1000002)_{10}$ e) We can't compare these numbers because at least one of them is invalid.
Problem 2 (1 Point)	<p>When a computer, using 2's complement system, performs the operation $(S = -2 - 3)$:</p> <ul style="list-style-type: none"> a) The computer will add two operands, which are $(0010)_2$ and $(0011)_2$ b) The computer will add two operands, which are $(1010)_2$ and $(1011)_2$ c) The computer will add two operands, which are $(0010)_2$ and $(1101)_2$ d) The computer will add two operands, which are $(1110)_2$ and $(0011)_2$ e) The computer will add two operands, which are $(1110)_2$ and $(1101)_2$
Problem 3 (1 Point)	<p>The Boolean expression $(A+B+C)(A'+B'+C')$ has a dual which is:</p> <ul style="list-style-type: none"> a) $(A'+B'+C')(A+B+C)$ b) $(A'+B'+C')+(A+B+C)$ c) $(A B C)(A' B' C')$ d) $(A B C) + (A' B' C')$ e) $A B C$
Problem 4 (1 Point)	<p>Given $F_1(A,B,C,D) = \Sigma(0, 2, 4, 8)$, $F_2(A,B,C,D) = \Sigma(1, 2, 3, 4, 15)$ and $F_3 = F_1 + F_2$ then:</p> <ul style="list-style-type: none"> a) $F_3(A,B,C,D) = \Sigma(2, 4)$ b) $F_3(A,B,C,D) = \Sigma(0, 1, 2, 3, 4)$ c) $F_3(A,B,C,D) = \Sigma(0, 1, 2, 3, 4, 8)$ d) $F_3(A,B,C,D) = \Sigma(0, 1, 2, 3, 4, 8, 15)$ e) $F_3(A,B,C,D) = \Sigma(5, 6, 7, 9, 10, 11, 12, 13, 14)$
Problem 5 (1 Point)	<p>The shown circuit can be implemented using a <u>minimum</u> of:</p> <ul style="list-style-type: none"> a) 3 NAND gates b) 4 NAND gates c) 4 NAND and 1 NOR gates d) 4 NAND and 2 NOR gates e) 5 NAND gates <div style="text-align: right;"> </div>

Problem 6 (1 Point)	<p>For the shown K-map, the simplified Boolean expression $F(A,B,C,D)$:</p> <p>a) 2 groups, each consisting of 4 squares b) 3 groups, each consisting of 4 squares c) 4 groups, each consisting of 4 squares d) 2 groups of 4 squares and 1 group of 2 squares e) 2 groups of 4 squares and 2 groups of 2 squares</p> 
Problem 7 (1 Point)	<p>The shown circuit is used to perform arithmetic functions on a 4-bit operand A, which is represented in 2's complement system, i.e. A can be positive or negative.</p> <p>a) $F = \begin{cases} A+1 & \text{if } C=0 \\ A-1 & \text{if } C=1 \end{cases}$ b) $F = \begin{cases} A-1 & \text{if } C=0 \\ A+1 & \text{if } C=1 \end{cases}$ c) $F = \begin{cases} A & \text{if } C=0 \\ A-1 & \text{if } C=1 \end{cases}$ d) $F = \begin{cases} A-1 & \text{if } C=0 \\ A & \text{if } C=1 \end{cases}$ e) $F = \begin{cases} A-1 & \text{if } C=0 \\ A-2 & \text{if } C=1 \end{cases}$</p> 
Problem 8 (1 Point)	<p>To implement the Boolean function $F = A \oplus B \oplus C$ we can use a 3-to-8 decoder and connect:</p> <p>a) 3 different lines from its output to an OR gate b) 4 different lines from its output to an OR gate c) 5 different lines from its output to an OR gate d) 6 different lines from its output to an OR gate e) 7 different lines from its output to an OR gate</p>
Problem 9 (1 Point)	<p>Computers “A” wants to transmit 8 bits of data to computer “B” using 8 wires. To be able to detect errors, we should use:</p> <p>a) 1 odd parity generator and 1 even parity checker, without adding any more wires. b) 1 odd parity generator and 1 odd parity checker, without adding any more wires. c) 1 odd parity generator and 1 even parity checker using 1 extra wire. d) 1 odd parity generator and 1 odd parity checker using 1 extra wire. e) 8 odd parity generators and 8 odd parity checkers using 8 extra wires.</p>
Problem 10 (1 Point)	<p>To “set” the shown latch, we should apply:</p> <p>a) $X = 1, Y = 0$ and $Z = 0$ b) $X = 1, Y = 1$ and $Z = 0$ c) $X = 0, Y = 1$ and $Z = 0$ d) $X = 0, Y = 1$ and $Z = 1$ e) $X = 1, Y = 0$ and $Z = 1$</p> 
Problem 11 (1 Point)	<p>The correct state diagram for the shown circuit is:</p> <p>a)  b)  c)  d) </p> 

Problem 12 (1 Point)	<p>Two 'T' Flip-Flops, A and B, are used to implement the shown state diagram. To go from state "AB = 01" to "AB = 11" we need:</p> <p>a) $T_A = 0, T_B = 0$ b) $T_A = 0, T_B = 1$ c) $T_A = 1, T_B = 0$ d) $T_A = 1, T_B = 1$ e) $T_A = 1, T_B = x$ (x is don't care)</p> 
Problem 13 (1 Point)	<p>A Universal Shift Register, USR, is connected as shown. $S_1=1, S_0=1$ select the load operation. Initially $Q_3Q_2Q_1Q_0 = 1010$. <u>After</u> 2 clocks:</p> <p>a) $Q_3Q_2Q_1Q_0 = 0000$ b) $Q_3Q_2Q_1Q_0 = 1010$ c) $Q_3Q_2Q_1Q_0 = 0101$ d) $Q_3Q_2Q_1Q_0 = 1001$ e) $Q_3Q_2Q_1Q_0 = 1111$</p> 
Problem 14 (1 Point)	<p>A ripple counter is a counter that:</p> <p>a) works synchronous b) works asynchronous c) can be designed to work synchronously or asynchronously d) counts "up" synchronously and "down" asynchronously (or vice versa) f) counts "Binary" synchronously and "BCD" asynchronously (or vice versa)</p>
Problem 15 (1 Point)	<p>The ring counter is a counter that:</p> <p>a) counts binary up b) counts binary down c) counts binary up or down d) counts BCD up or down e) doesn't really count like a binary or BCD</p>



Solution Key

Problem	Answer
1-	(b)
2-	(e)
3-	(d)
4-	(d)
5-	(b)
6-	(a)
7-	(c)
8-	(b)
9-	(d)
10-	(d)
11-	(a)
12-	(c)
13-	(a)
14-	(b)
15-	(e)